FIG. 1 PRIOR ART

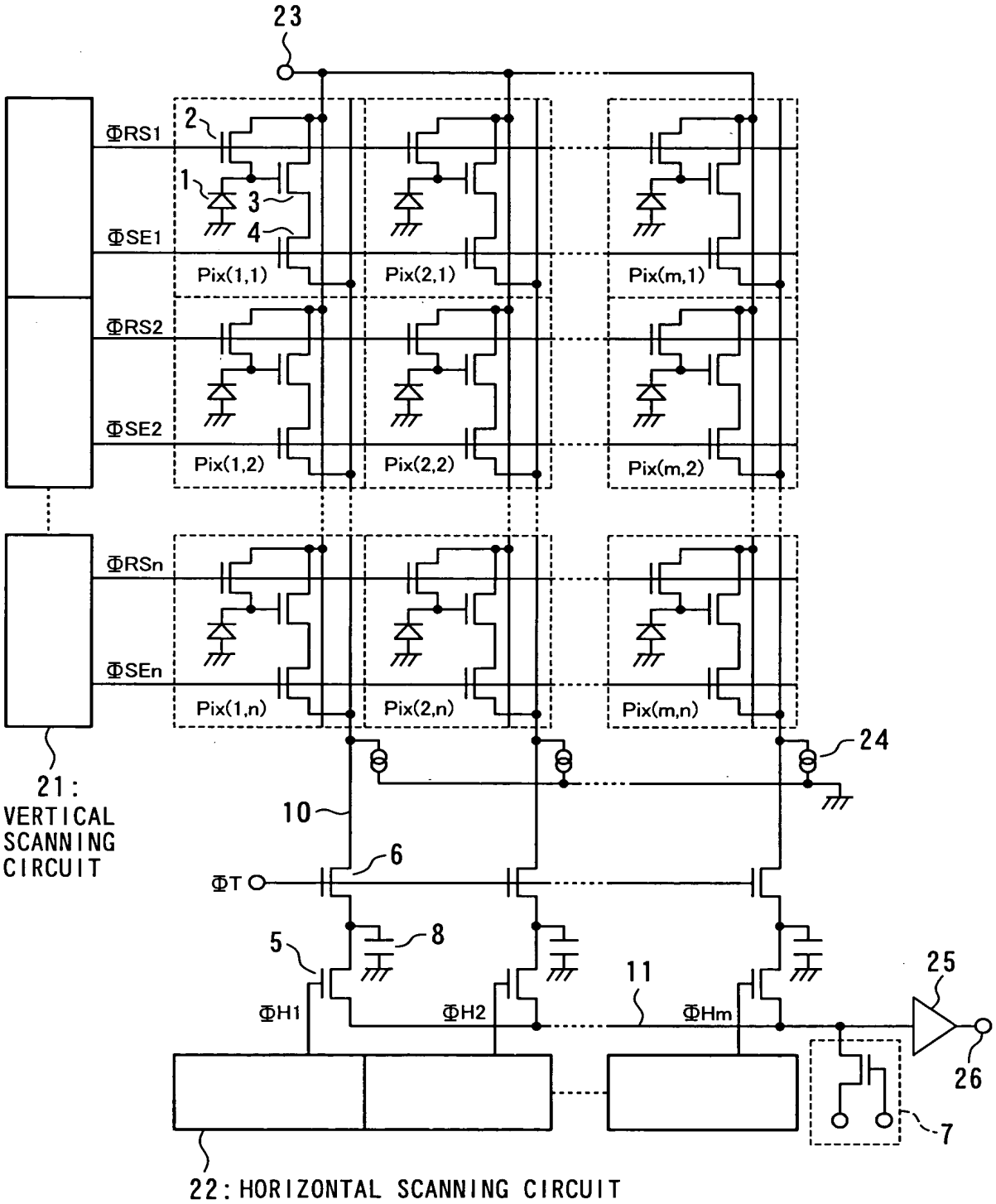


FIG. 2 PRIOR ART

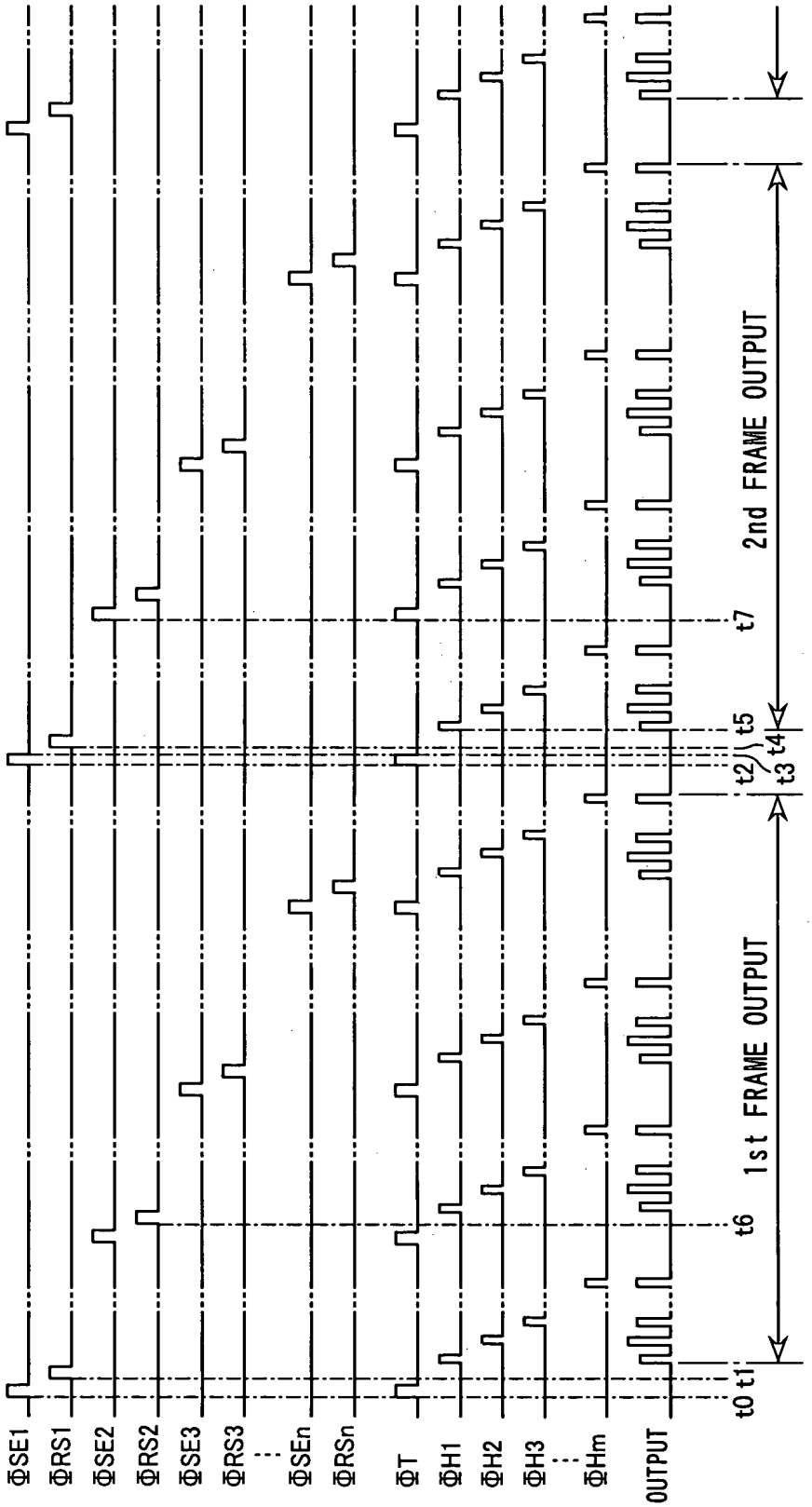


FIG. 3 PRIOR ART

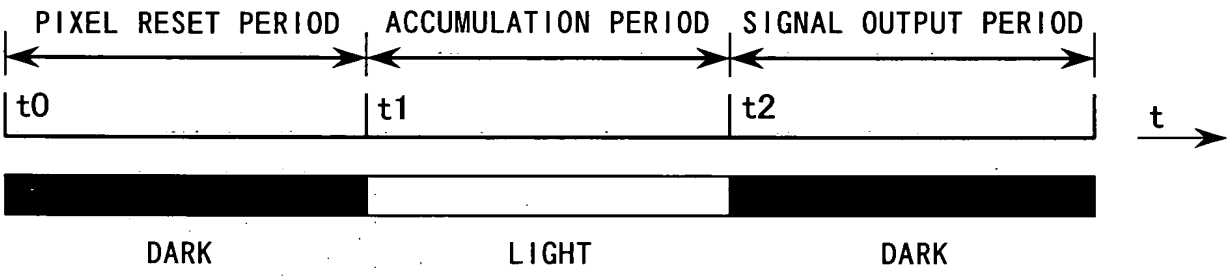


FIG. 4

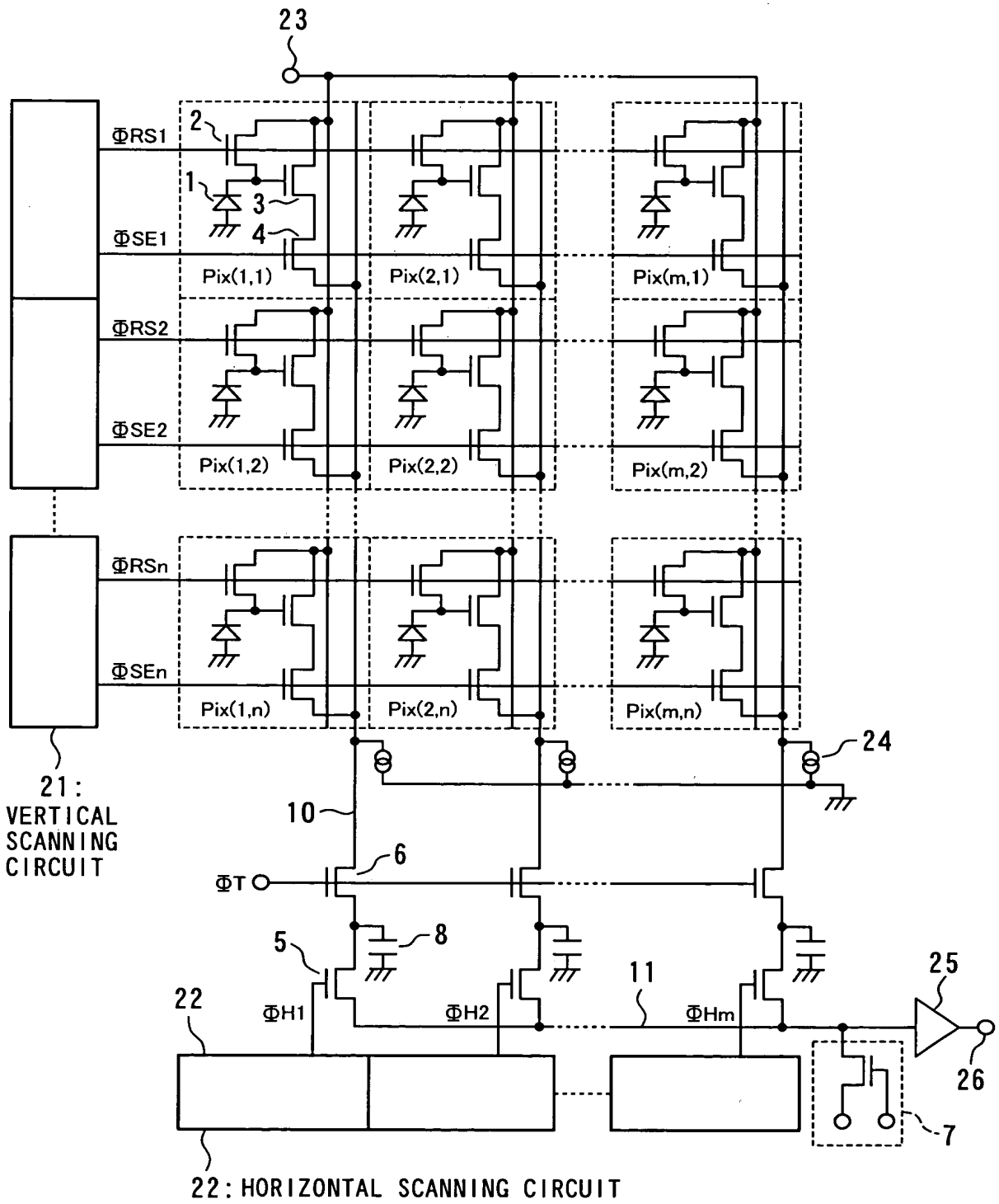

23
ΦRS1
ΦSE1
ΦRS2
ΦSE2
ΦRSn
ΦSEn
1
2
3
4
Pix(1,1)
Pix(2,1)
Pix(m,1)
Pix(1,2)
Pix(2,2)
Pix(m,2)
Pix(1,n)
Pix(2,n)
Pix(m,n)
21: VERTICAL SCANNING CIRCUIT
24
10
6
ΦT
5
8
11
25
22
ΦH1
ΦH2
ΦHm
26
7
22: HORIZONTAL SCANNING CIRCUIT

FIG. 5

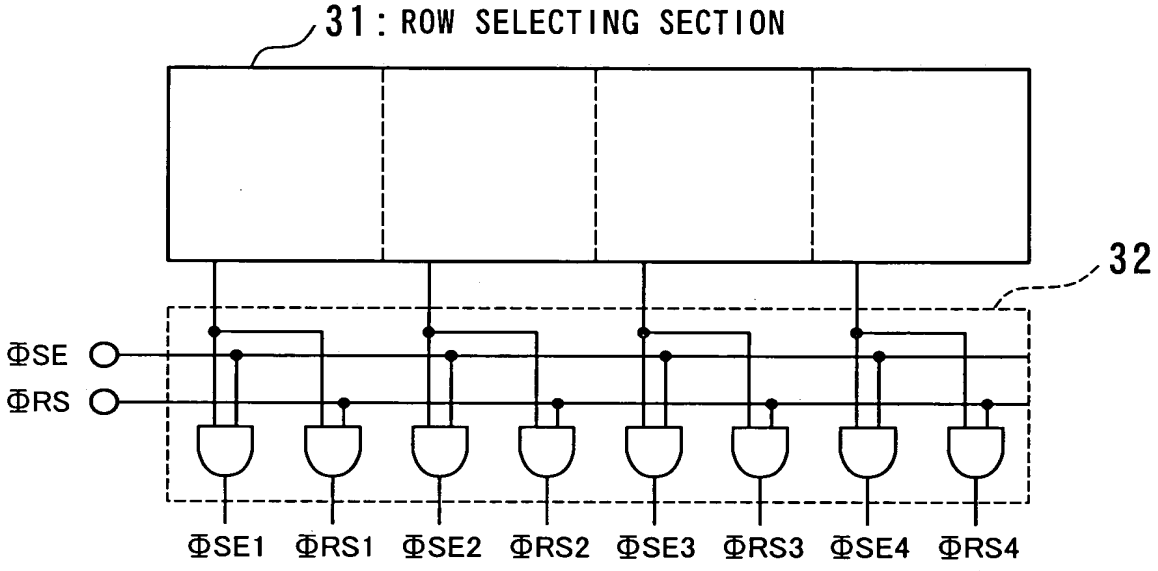
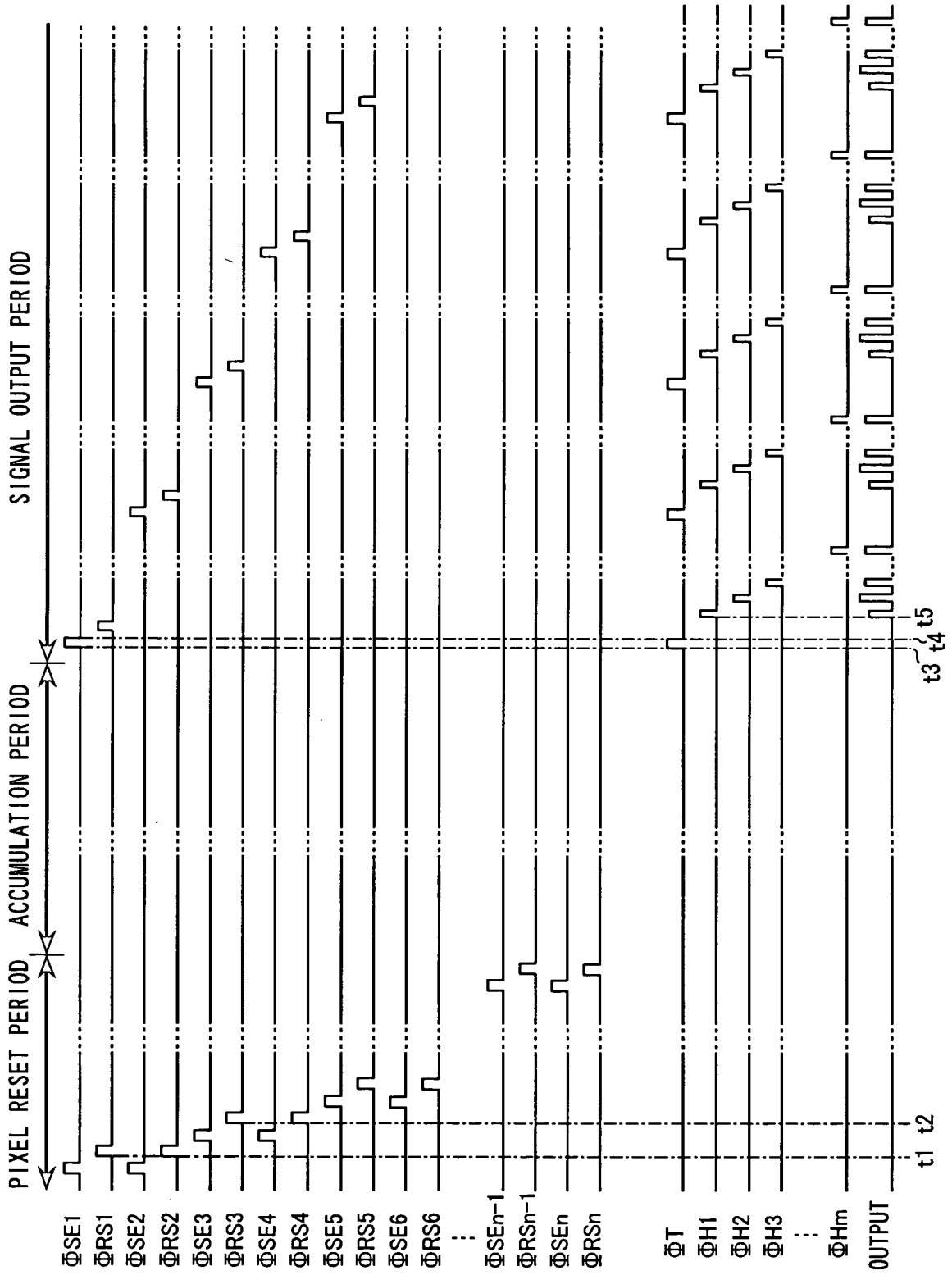

31 : ROW SELECTING SECTION
32
ΦSE
ΦRS
ΦSE1
ΦRS1
ΦSE2
ΦRS2
ΦSE3
ΦRS3
ΦSE4
ΦRS4

FIG. 6


PIXEL RESET PERIOD
ACCUMULATION PERIOD
SIGNAL OUTPUT PERIOD
ΦSE1
ΦRS1
ΦSE2
ΦRS2
ΦSE3
ΦRS3
ΦSE4
ΦRS4
ΦSE5
ΦRS5
ΦSE6
ΦRS6

ΦSEn-1
ΦRSn-1
ΦSEn
ΦRSn
ΦT
ΦH1
ΦH2
ΦH3

ΦHm
OUTPUT
t1 t2
t3 t4 t5

FIG. 7

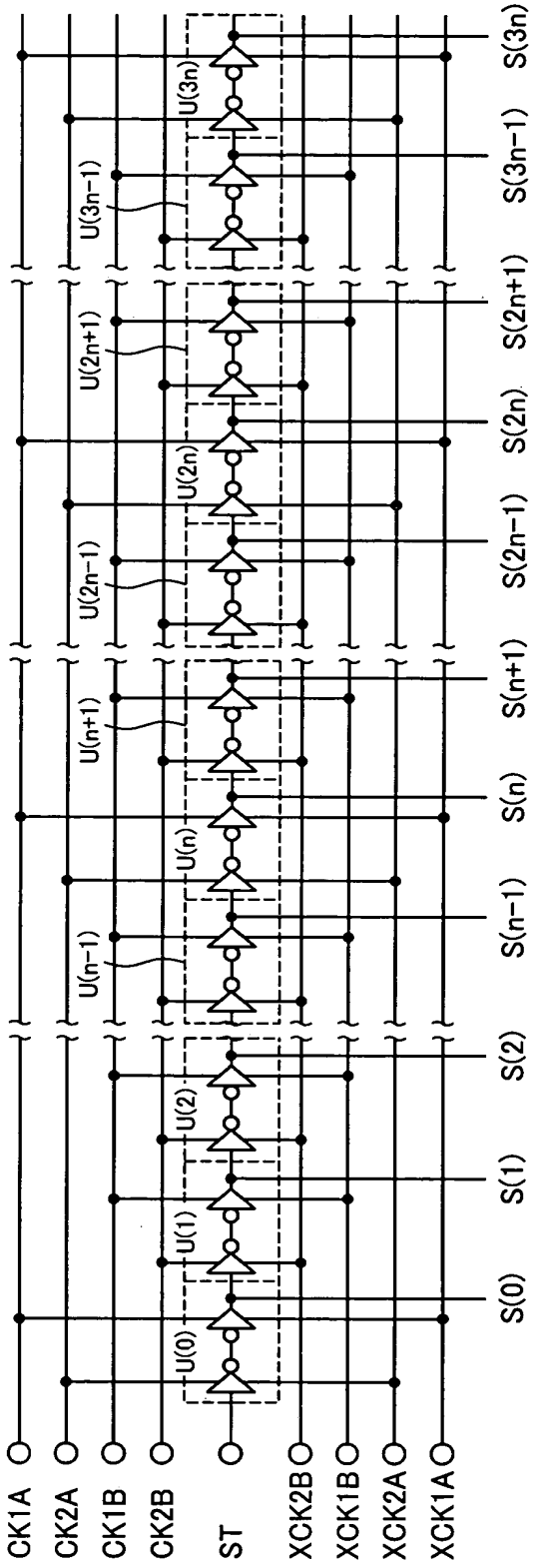

CK1A
CK2A
CK1B
CK2B
ST
XCK2B
XCK1B
XCK2A
XCK1A
U(0)
U(1)
U(2)
U(n-1)
U(n)
U(n+1)
U(2n-1)
U(2n)
U(2n+1)
U(3n-1)
U(3n)
S(0)
S(1)
S(2)
S(n-1)
S(n)
S(n+1)
S(2n-1)
S(2n)
S(2n+1)
S(3n-1)
S(3n)

FIG. 8

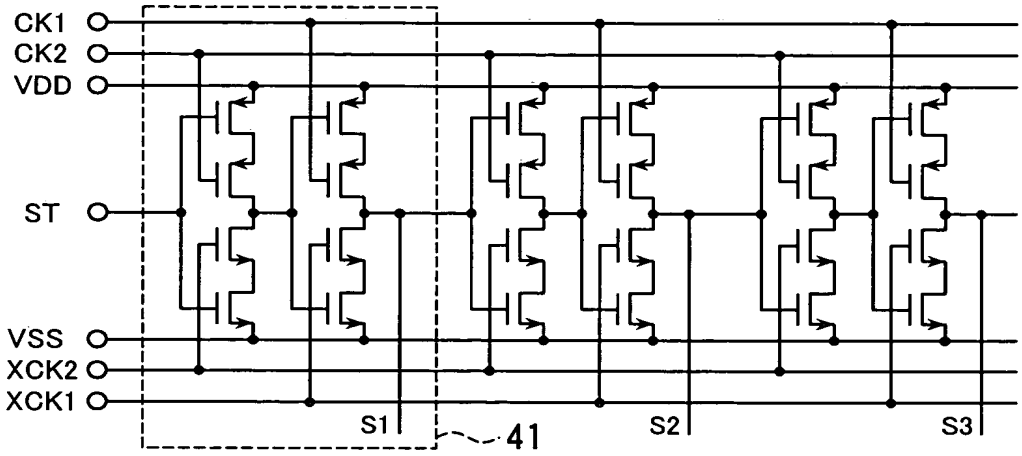

CK1
CK2
VDD
ST
VSS
XCK2
XCK1
S1
41
S2
S3

FIG. 9

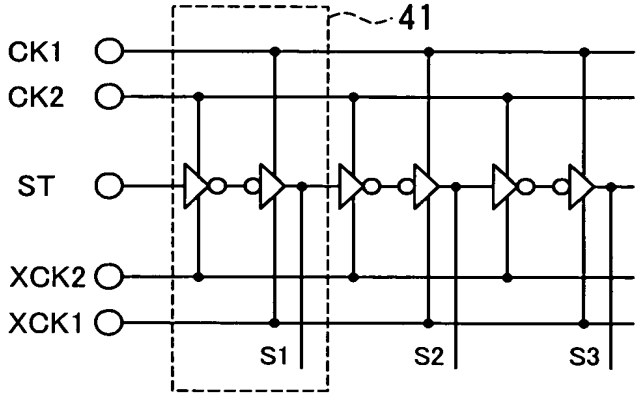

41
CK1
CK2
ST
XCK2
XCK1
S1
S2
S3

FIG. 10

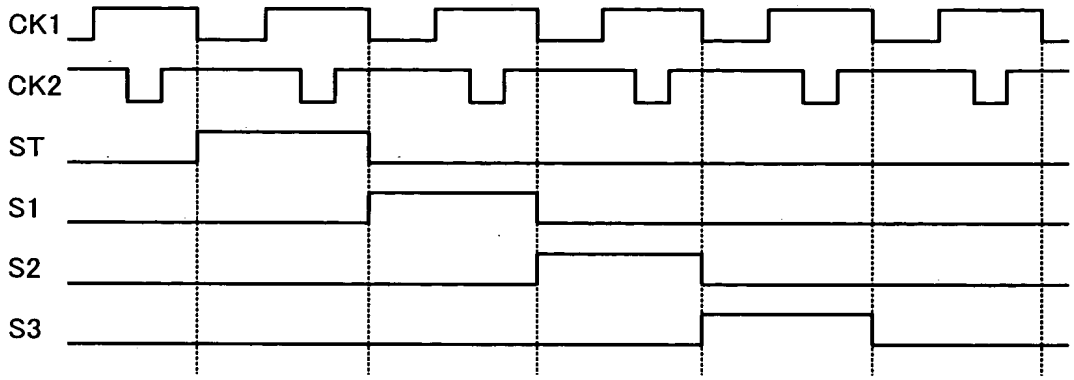


FIG. 11

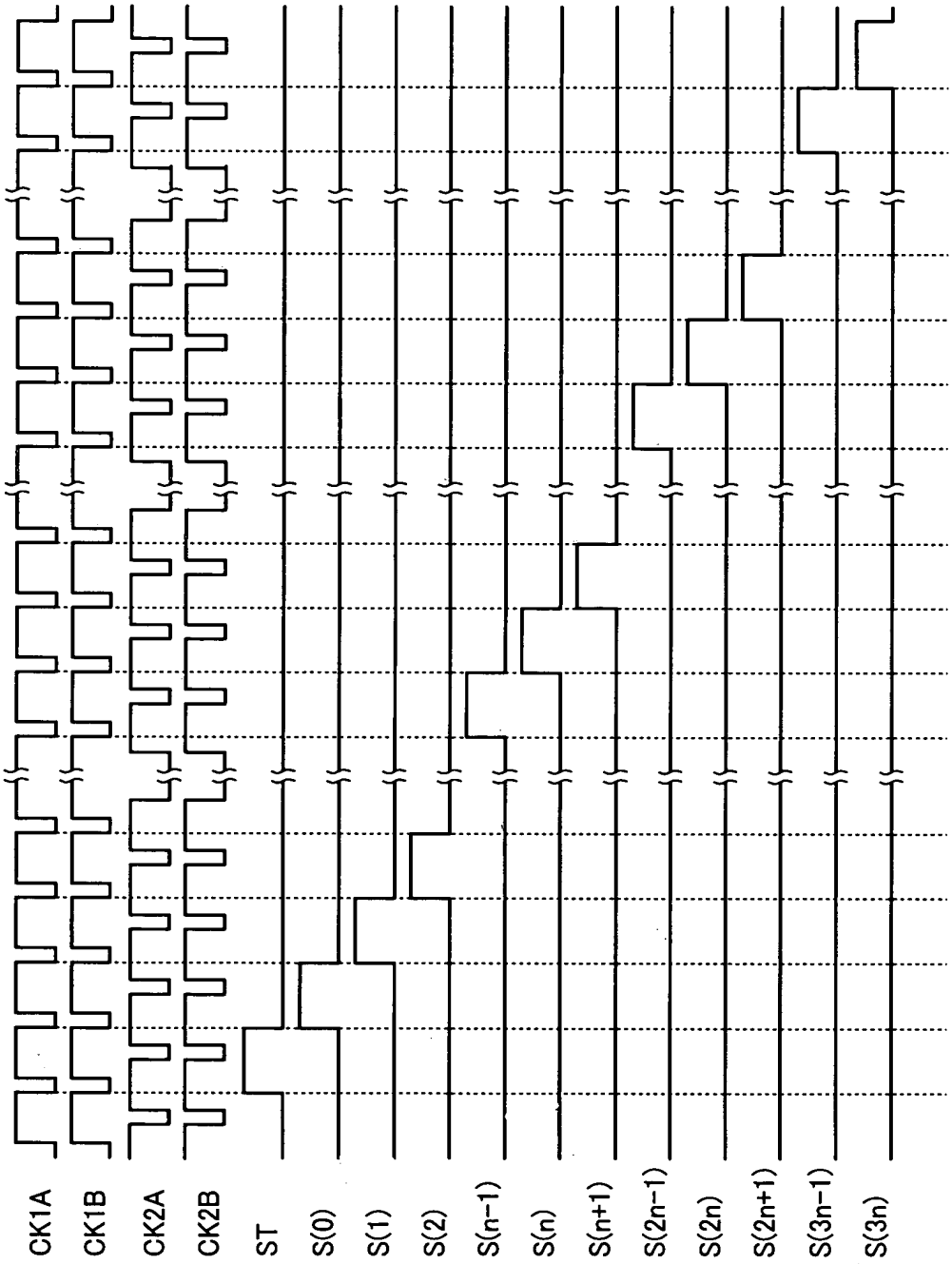

CK1A
CK1B
CK2A
CK2B
ST
S(0)
S(1)
S(2)
S(n-1)
S(n)
S(n+1)
S(2n-1)
S(2n)
S(2n+1)
S(3n-1)
S(3n)

FIG. 12

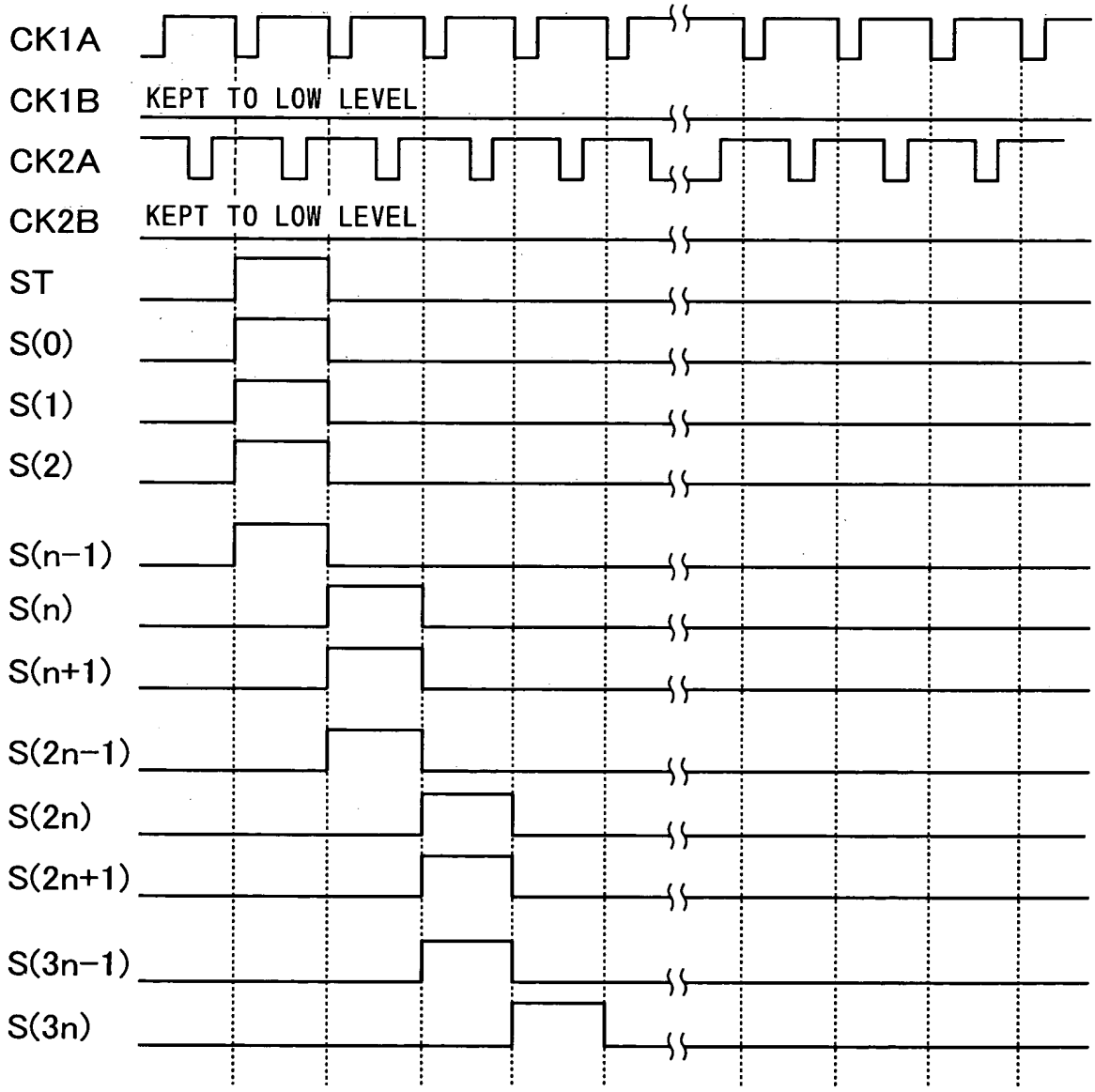

CK1A
CK1B
KEPT TO LOW LEVEL
CK2A
CK2B
KEPT TO LOW LEVEL
ST
S(0)
S(1)
S(2)
S(n−1)
S(n)
S(n+1)
S(2n−1)
S(2n)
S(2n+1)
S(3n−1)
S(3n)

FIG. 13

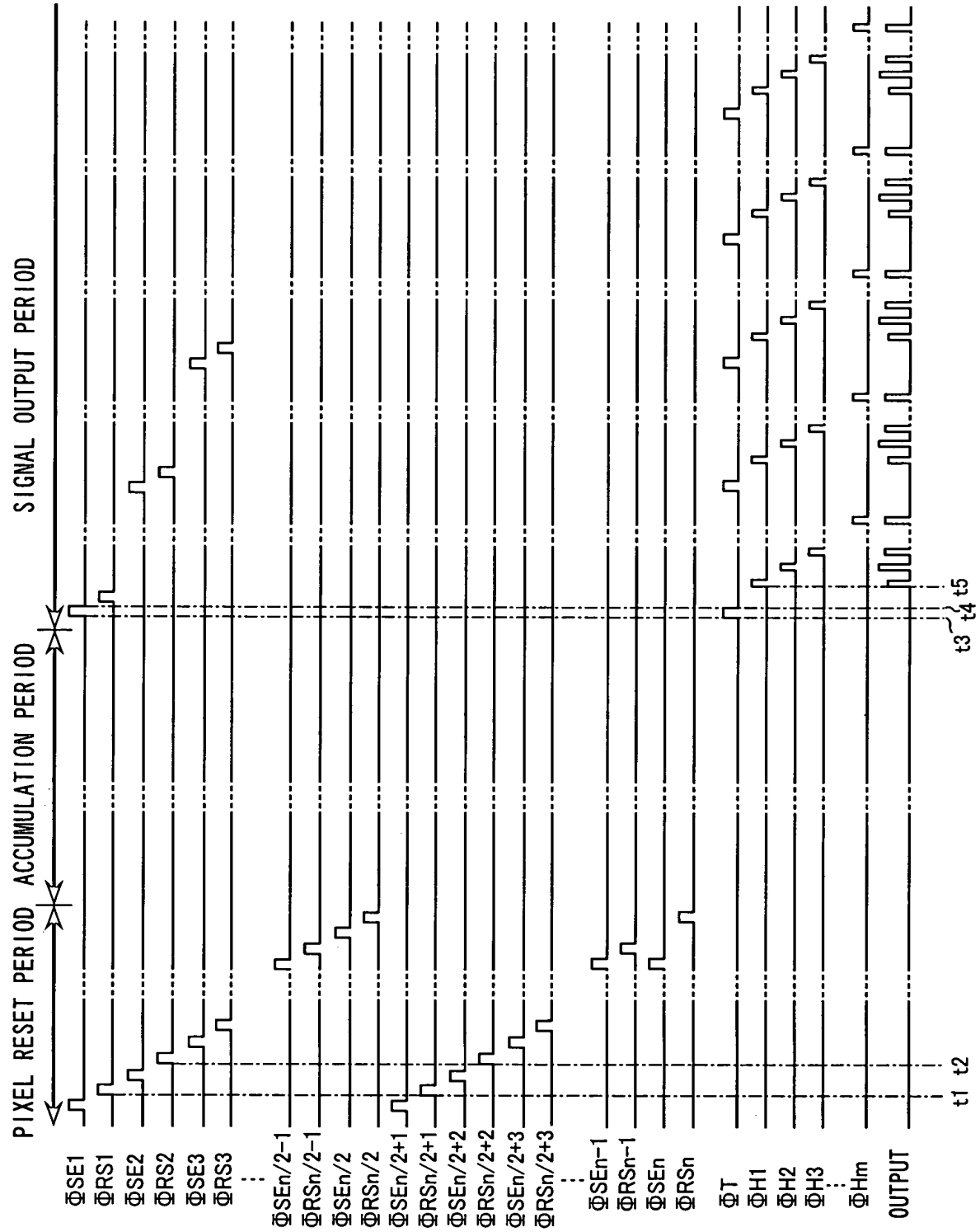

PIXEL RESET PERIOD
ACCUMULATION PERIOD
SIGNAL OUTPUT PERIOD
ΦSE1
ΦRS1
ΦSE2
ΦRS2
ΦSE3
ΦRS3
ΦSEn/2-1
ΦRSn/2-1
ΦSEn/2
ΦRSn/2
ΦSEn/2+1
ΦRSn/2+1
ΦSEn/2+2
ΦRSn/2+2
ΦSEn/2+3
ΦRSn/2+3
ΦSEn-1
ΦRSn-1
ΦSEn
ΦRSn
ΦT
ΦH1
ΦH2
ΦH3
ΦHm
OUTPUT
t1 t2
t3 t4 t5

FIG. 14

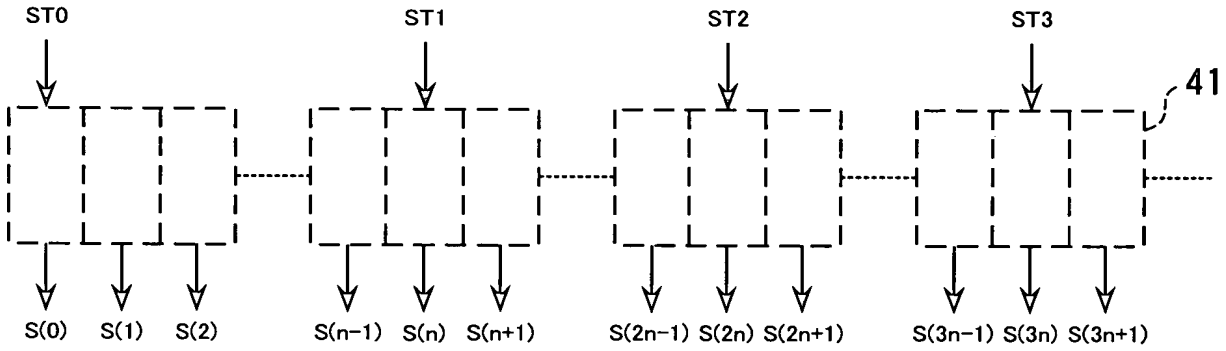
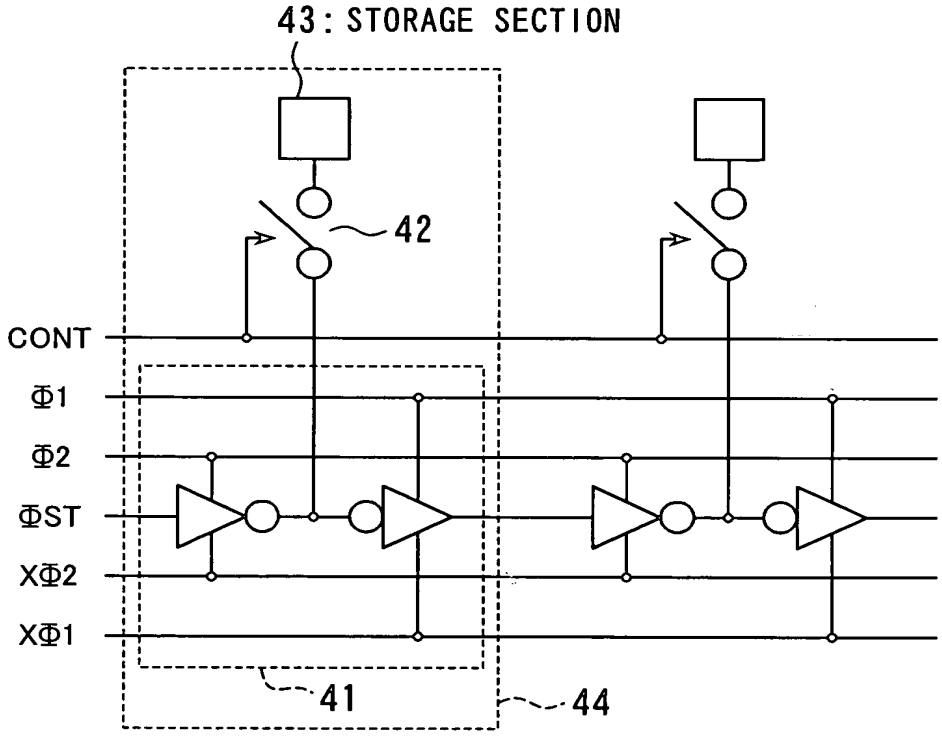

ST0
ST1
ST2
ST3
41
S(0)
S(1)
S(2)
S(n-1)
S(n)
S(n+1)
S(2n-1)
S(2n)
S(2n+1)
S(3n-1)
S(3n)
S(3n+1)

FIG. 15


43: STORAGE SECTION
42
CONT
Φ1
Φ2
ΦST
XΦ2
XΦ1
41
44